Low latency, high throughput network-on-chip for multiprocessors

Technology #m11-080

Network-on-chip (NOC) technology has allowed for the incorporation of several IP cores onto a single integrated circuit chip. However, recent studies have pointed to performance shortcomings that may occur using current NOC technology as the electronics industry continues to push for hardware scalability. Removal of the internal global clock has yielded both fully asynchronous and globally-asynchronous locally-synchronous (GALS) NOC systems, which offer the potential of lower system latency, reduced power consumption, higher performance, and increased flexibility in heterogeneous component integration. This technology is an asynchronous NOC system that makes use of bi-modal arbitration nodes to achieve improvements in system latency and throughput. A specialized node architecture permits dynamic reconfiguring based on the amount of traffic received, leading to improvements in node latency and throughput. Use of this node architecture within a NOC system may thus lead to high-performance, asynchronous networking for shared-memory chip multiprocessors.

Bi-modal arbitration node supports single-channel-bias to improve node latency and cycle time

The bi-modal arbitration node switches to “single-channel bias” mode when one of its two input channels is inactive, allowing for decreased latency and increased throughput within the active channel, even under high traffic. The node is then switched back to its traditional mode when signals are detected at both inputs. Since the switching operation requires very little overhead, this process can be performed dynamically in response to widely varying levels of local input traffic. The target network topology for this technology is a variant Mesh-of-Trees, which provides the needed bandwidth for high-performance parallel processors with globally uniform memory access. Furthermore, this technology can be implemented as a fully asynchronous network or using GALS systems.

SPICE simulations were used to compare this technology to conventional asynchronous NOCs on the basis of eight benchmarks. NOCs using the bi-modal arbitration nodes exhibited improvements in system latency up to 19.8% and throughput up to 27.8%.

Lead Inventor:

Steven Nowick, Ph.D.
Applications:

- Asynchronous networking for chip multiprocessors
- Network-on-chip design
- Circuit primitive construction

Advantages:

- Decreased latency and increased throughput
- Can be implemented using a fully asynchronous or GALS NOC system
- Tailored for a Mesh-of-Trees network

Patent Information:

Patent Pending (US 20140341443)

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Related Publications:


Inventors

Steven Nowick