A method to reduce integrated circuit size by placing additional elements beneath an inductor

As CMOS circuits continue to miniaturize, analog circuit elements such as inductors and capacitors are unable to scale at the same rate while maintaining quality. In an effort to reduce overall circuit size, this technology offers a method to place parts of a circuit beneath an inductor coil, reducing circuit size by about 50%. This efficient use of space allows for a more diverse range of miniaturized devices such as RFID tags.

By carefully planning current paths and magnetic coupling between the inductor and the circuit, eddy currents can be reduced keeping the quality of the circuit at a high level

Using a phase-locked loop (PLL) design, the capacitor is placed underneath the inductor to save space and shield the inductor from the surrounding circuit currents. Along with carefully planned current paths and magnetic coupling, this design allows for a high quality factor for the inductors while reducing the size of the circuit by about 50%.

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Applications:

• Reducing the size of integrated circuit designs
• Because of size reduction, the technology could be used in RFID tags for wireless entry or communication

Advantages:

• Analog devices can be further miniaturized while the level of inductor quality is maintained
• Inductors can be incorporated in to a more diverse array of miniaturized electronics
Patent information:

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Related Publications:

• Zhang, F., Chu, C.F., Kinget, P. Voltage-controlled oscillator in the coil. IEEE Xplore. Sept. 2005

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