Low Latency FIFO Circuits for Mixed Asynchronous and Synchronous Systems

“Name of the inventor: Tiberiu Chelcea FIFO Circuit Design for Synchronous or Asynchronous Speeds A system for low latency FIFO circuit design. These circuits can interface with subsystems working at different speeds and can be synchronous or asynchronous. FIFO Circuit System with Low Latency and High Throughput A circuit which interfaces the transmission of a data item from an asynchronous sender subsystem to a synchronous receiver subsystem includes a chain of relay stations. The relay stations are attached to the sender subsystem to transmit the data item on a put data bus. A relay station receives a clock signal and transmits the data item from the relay stations. An empty detector in the relay station produces an empty control signal synchronized with the clock signal. De-queuing of a data item is enabled on each clock cycle if the empty signal is asserted.

The system provides a FIFO circuit having low latency and high throughput and capable of operation in mixed synchronous/asynchronous environments.”

Inventors

Steven Nowick