Low latency FIFO circuits for mixed asynchronous and synchronous systems

Technology #m00-060

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A FIFO design that interfaces a sender subsystem and a receiver subsystem operating on different time domains are described.

The FIFO circuit comprises of a put interface is configured to operate according to a protocol of operation. A put circuit and get circuit comprises of a put/get data bus to transmit a data item from the sender subsystem and a put/get data request input to receive the put/get request. An array of cells is provided in which each cell has a register configured to receive the data item from the put data bus and to transmit the data item to the get data bus. A state controller provides an indication of the state of the cell. A put/get component receives the put/get token from an adjacent cell and latches the data item received from the put/get data bus to the register based on the put/get request. The put/get token is then passed to the adjacent cell.

A FIFO circuit having low latency and high throughput and capable of operation in mixed synchronous/ asynchronous environments.

Inventors

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